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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,535	04/09/2001	Yu-Chin Hsu	NOVA 2198	8462

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,535	HSU ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) *5 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-16 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 were presented for examination and rejected in non-final office action August 24, 2004. A discrepancy between the claim listing and the amended claims was clarified via phone interview on March 30, 2005. Claims 1-4, 6-16, and 18-24 have been amended and are currently pending in the instant application. An interview summary is attached.

Response to Remarks

Regarding sections 1 and 2 of the previous office action regarding objections to the specification, the Examiner thanks Applicant for amending in response to those objections. Those objections have been withdrawn.

Rejections under 35 U.S.C. § 102

In response to the rejections of claims 1-24 under 35 U.S.C. § 102(b) as anticipated by US Patent No. 5,220,512 to Watkins et al. (Watkins), Applicant primarily argues (page 16):

> Thus the array of register symbols includes basically the same information as the state table of WATKINS' FIG. 4.
> However the applicant's display also includes a plurality of graphic symbols (lines), each visually linking one register symbol in one column corresponding to one time to other register symbols in another column corresponding to one time to other register symbols in another column corresponding to a preceding time.

Applicant exemplifies this argument with reference to FIG. 10 of the instant application.

Applicant's further argues that the amended claim language recites this display, exemplified in the arguments for claim 1 (page 17):

> However claim 1 further recites "wherein the display also includes a graphical representation of a logical relationship depicted by one of the net models visually linking one register symbol of the register symbols residing in one of the columns to other register symbols residing in another of the columns, and wherein the graphical representation indicates that a register output signal state indicated by the one register symbol, and states of register output signals indicated by theother register symbols are logically interrelated".

The Examiner has given these arguments due consideration and concedes that the Watkins reference alone does neither teach nor make obvious the display recited by the amended limitations of claim 1. However, the Examiner emphasizes that "the array of register symbols [of Applicant's invention] includes basically the same information as the state table of Watkins' FIG. 4", as put forth by Applicant. The difference between Watkins' invention, exemplified by FIG. 4, and Applicant's invention is found in the amended limitations regarding Applicant's particular display of "basically the same information".

An updated search of the prior art has uncovered references that teach the display recited by the amended claim language.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1-4, 6-16, and 18-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by US Patent No. 6,789,242 to Liu.

3. Regarding claims 1, 12, 13 and 24 Liu teaches a verification tool to simulate the performance of a circuit design of a period of time, including the signal values on carried on input lines within the circuit (column 4, lines 40-58).

Although Liu does not explicitly recite a step of generating a plurality of net models, Liu does state "the designer can use the verification tool to specify a storage element and request the tool to display the signal value on an output line coupled to the specified storage element at a time-frame t" (column 4, lines 42-46) and "The verification tool displays the signal values carried on the input lines coupled to the input of the specified storage element at time-frame t-1" (column 4, lines 48-51). It is inherent that when a designer, through normal use of the verification tool, performs the step of specifying a storage element (a register) more than once, the verification tool generates a plurality of net models as recited by claim 1.

Liu teaches a display (exemplified by FIG. 5) wherein a circuit with three consecutive levels of storage (three levels of registers) that teach the recited display of claim 1 (column 7, lines 39-53). Most notably, the registers (represented in FIG. 5 using standard symbology for circuit schematics) are annoted with a digital value (0 or 1 in FIG. 5) and an indication of the time frame, equivalent to a "time" as recited by claim 1 ((t8), (t7), et cetera in FIG. 5). The display clearly includes a graphical representation of

a logical relationship between the registers, visually linking register symbols at different time frames with lines. Thus the registers are represented at different times, the states of the register symbols are represented, and the register symbols are visually linked.

Liu teaches that the register symbols are loosely arranged into columns, as indicated in FIG. 5 by the vertical dashed lines and further by labeling the areas demarcated by the dashed lines to correspond to particular time frames ((t5), (t6), et cetera, at top of the FIG. 5).

4. Regarding claims 2 and 14, Liu teaches that the state of the register output signal indicated by the one register symbol is a function of the state of the register output signals indicated by the other register symbols (FIG. 5). In FIG. 5, register 307 has an output state of 0 at time 8 (t8). This output state is the function of registers 304, 305, and 306 and the accompaning digital logic 309, 310, 314, and 312, as represented by the schematic.

5. Regarding claims 3 and 15, Liu teaches a feature of the verification tool which causes the tool to "display a first signal value carried on the first signal signal line at the first time-frame; display a second signal value carried on the second signal line at the second time-frame; and display a third signal value carried on the third signal line at the third time-frame" (column 3, lines 43-49). This feature is exemplified by FIGS. 6D and 6E, clearly depicting the forward propagation of a signal value stored at, for example, register 602' starting at time-frame (t5) and ending with time-frame (t8).

6. Regarding claims 4 and 16, Liu teaches that the display includes symbols that represent signal inputs (FIG. 5, represented as "1 (t5)" at the left edge of the figure). The schematic of FIG. 5 clearly links the input symbols to the registers.

7. Regarding claims 6 and 18, Liu teaches that the register output signal state indicated by the one register symbol is a logical function of states of register output signals indicated by the other register symbols and the state of at least one of the circuit input signals (FIG. 5). The schematic and associated circuit elements convey the logical function of the other registers using well known and industry standard symbology.

8. Regarding claims 7 and 19, Liu teaches that a graphical representation of a logical relationship comprises visually linking register symbols in different columns (FIG. 5). The schematic and associated circuit elements are linked using lines to represent logical connections within the circuit.

9. Regarding claims 8 and 20, Liu teaches that the graphical representation of the logical relationship also comprises the visually linking circuit logic depicted by at least one of a plurality of logic gate symbols to the one register symbol (FIG. 5). Logic gate symbols 309, 312, and 314 are clearly linked to register symbol 307.

10. Regarding claims 9 and 21, Liu teaches that the representation of a logical relationship comprises lines interconnecting the one register symbol to the other register symbols and at least one of the circuit input signal symbols (FIG. 5). The schematic comprising lines representing logical connections within the circuit and associated circuit elements convey the logical function of the other registers using well known and industry standard symbology.

11. Regarding claims 10 and 22, Liu teaches a graphical representation of a logical relationship comprising a graphical representation of a net model visually linking the circuit input signals and other register symbols to a register input signal symbol depicting a state of a register input signal (FIG. 5, entire figure).

12. Regarding claims 11 and 23, Liu teaches a graphical representation visually linking the other register symbols to the one register symbol indicates a changed state of the other register symbol after being clocked by a clock signal edge at a time corresponding to a column in which the other symbol resides (FIG. 5). For example, the input of register 304 at time-frame 6 (t6) is 0, indicated by the output of logic gate 313. At time-frame 7 (t7), register 304's output signal is therefore 0, as shown.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding

the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
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